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Paper 45
Date: March 18, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD
AND
INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

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IPR2023-01381
Patent 8,350,294 B2

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Before JON B. TORNQUIST, JEFFREY W. ABRAHAM, and KIMBERLY McGRAW, *Administrative Patent Judges*.

TORNQUIST, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
Granting Patent Owner's Motion to Amend
*35 U.S.C. § 318(a)*

## I. INTRODUCTION

Innoscience (Zhuhai) Technology Company, Ltd. and Innoscience America, Inc. (collectively "Petitioner") filed a Petition requesting *inter partes* review of claims 1–12 of U.S. Patent No. 8,350,294 B2 (Ex. 1001, "the '294 patent"). Paper 1 ("Pet."). Efficient Power Conversion Corporation ("Patent Owner") filed a Preliminary Response to the Petition. Paper 7. With authorization, Petitioner subsequently filed a Preliminary Reply (Paper 8) and Patent Owner filed a Preliminary Sur-reply (Paper 10).

Upon review of the parties' arguments and supporting evidence, we instituted review with respect to all grounds and claims set forth in the Petition. Paper 11. After institution, Patent Owner filed a Response (Paper 18, "PO Resp."), to which Petitioner filed a Reply (Paper 26, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 32, "Sur-reply").

Patent Owner also filed a non-contingent Motion to Amend (Paper 17, "Mot."), to which Petitioner filed an Opposition (Paper 27, "Opp."), Patent Owner filed a reply (Paper 31, "Mot. Reply"), and Petitioner filed a sur-reply (Paper 37, "Mot. Sur-reply"). In its Motion to Amend, "Patent Owner requests that claims 4–6 and 10–12 be cancelled and that proposed new claims 13–14 be entered." Mot. 1. As Patent Owner's request to cancel claims 4–6 and 10–12 is non-contingent, only original claims 1–3 and 7–9 remain in this proceeding. *Id.*

On October 1, 2024, the Board issued Preliminary Guidance with respect to Patent Owner's Motion to Amend. Paper 29.

In support of their respective arguments, Petitioner relies, *inter alia*, upon three declarations from James Richard Shealy, Ph.D. (Ex. 1003 (original declaration); Ex. 1033 (supplemental declaration); Ex. 1039 (supplemental declaration addressing the Motion to Amend)), and Patent

Owner relies upon two declarations from E. Fred Schubert, Ph.D. (Ex. 2009 (original declaration); Ex. 2024 (supplemental declaration addressing the Motion to Amend)).

An oral hearing was held on December 18, 2024, and a transcript of the hearing is included in the record (Paper 44, "Tr.").

For the reasons that follow, we conclude that Petitioner demonstrates by a preponderance of the evidence that claims 1–3 and 7–9 are unpatentable. Petitioner has not demonstrated by a preponderance of the evidence, however, that proposed substitute claims 13 and 14 are unpatentable.

## II. BACKGROUND

### *A. Related Matters*

The parties indicate that the '294 patent is at issue in the following proceedings: (1) *Efficient Power Conversion Corporation v. Innoscience (Zhuhai) Technology Co., Ltd.*, 2:23-cv-04026-AB-AS (C.D. Cal.), and (2) *Certain Semiconductor Devices, and Methods of Manufacturing Same and Products Containing the Same*, 337-TA-1366 (USITC). Pet. 90; Paper 5, 2.

### *B. Real Parties in Interest*

Petitioner identifies itself (the two parties identified in the caption) and Innoscience (Suzhou) Technology Company, Ltd. as the real parties-in-interest. Pet. 90. Patent Owner identifies itself as the real party-in-interest. Paper 5, 1–2.

### *C. The '294 Patent*

The '294 patent is titled "Compensated Gate MISFET and Method for Fabricating the Same" and issued January 8, 2013. Ex. 1001, codes (45),

(54). The '294 patent is directed to the "field of enhancement mode gallium nitride (GaN) transistors" and, in particular, to "an enhancement mode GaN transistor with a compensated GaN layer or a semi-insulating GaN layer below the gate contact and above the barrier layer." *Id.* at 1:13–17.

The '294 patent explains that a GaN high electron mobility transistor (HEMT) includes a nitride semiconductor with at least two nitride layers. Ex. 1001, 1:30, 34–35. "Different materials formed on the semiconductor or on a buffer layer causes the layers to have different band gaps," and the "different material in the adjacent nitride layers also causes polarization, which contributes to a conductive two dimensional electron gas (2DEG) region near the junction of the two layers." *Id.* at 1:35–40. "Because the 2DEG region exists under the gate at zero gate bias, most nitride devices are normally on, or depletion mode devices." *Id.* at 1:45–47. "If the 2DEG region is depleted, i.e. removed, below the gate at zero applied gate bias," however, "the device can be an enhancement mode device," which is normally off. *Id.* at 1:47–50. The '294 patent explains that enhancement mode devices are desirable due to their increased safety and the ability to control such devices "with simple, low cost drive circuits." *Id.* at 1:50–53.

Figure 1 of the '294 patent is reproduced below.

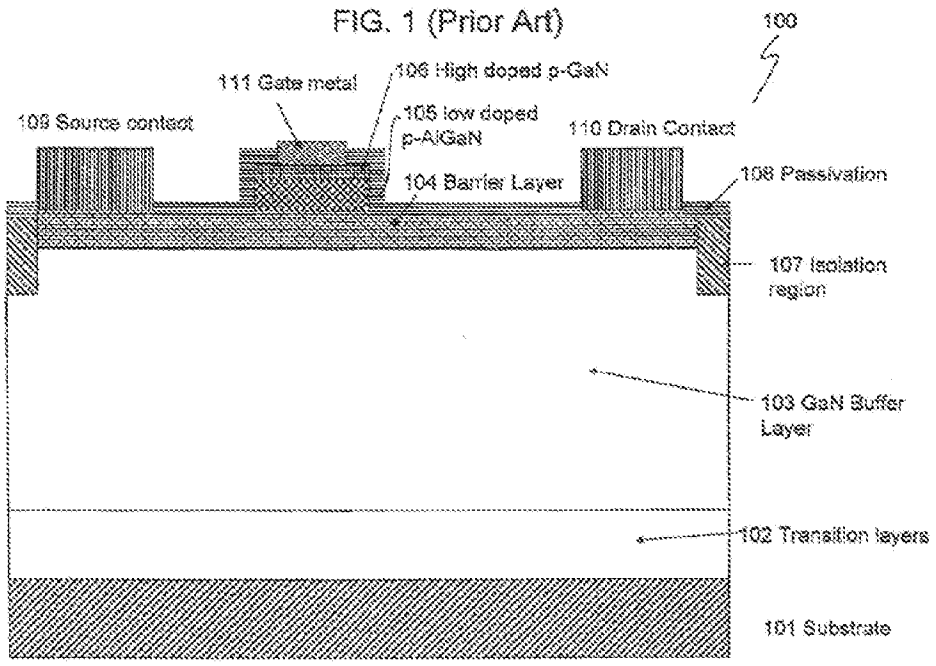



Figure 1 is a cross-section of a conventional enhancement mode GaN transistor device 100. Ex. 1001, 1:55–56, 2:23. As shown in Figure 1, transistor device 100 includes substrate 101, transition layers 102, buffer material 103 (typically composed of GaN), barrier material 104 (typically composed of AlGaN), p-type AlGaN layer 105, heavily doped p-type GaN layer 106, isolation region 107, passivation region 108, ohmic contact metals 109 and 110 (source and drain, respectively), and gate metal 111 (typically composed of nickel and gold) that resides over the p-type GaN gate. *Id.* at 1:56–2:2. The '294 patent reports that this conventional GaN transistor has several disadvantages, including "very high" "leakage current of the gate contact during device conduction" due to gate charge injection, as well as capacitance between the gate electrode and channel layer. *Id.* at 2:3–6, 3:50–52.

Figure 2 of the '294 patent is reproduced below.

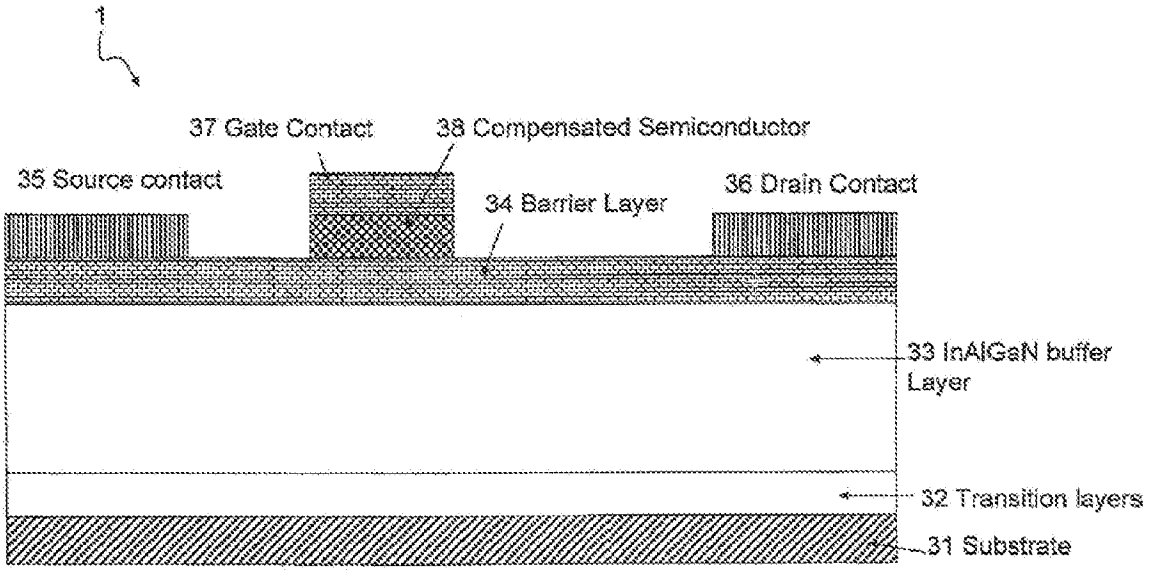



Figure 2 shows a MISFET (metal insulator semiconductor field effect transistor) in the form of an enhancement mode GaN transistor 1. Ex. 1001, 2:24–25, 2:56–57. Transistor 1 is formed on substrate 31, which may be, for example, silicon, silicon carbide, or sapphire. *Id.* at 2:57–59. "Over and in contact with the substrate 31 are transition layers 32." *Id.* at 2:59–60. Buffer layer 33 separates transition layers 32 from barrier layer 34 and is preferably formed of InAlGaN. *Id.* at 2:62–64. Source contact 35 and drain contact 36 are disposed over barrier layer 34. *Id.* at 3:1–2. Gate contact 37 is provided between the source and drain contacts. *Id.* at 3:4–7. Compensated semiconductor layer 38 is formed over barrier layer 34 and under gate contact 37 and preferably comprises "AlGaN or GaN with a deep level passivated p-type impurity such as, for example, Mg, Zn, Be, Cd, or Ca." *Id.* at 3:7–12.

The '294 patent explains that "the high doping level of compensated layer 38 leads to enhancement mode devices," which "are normally off" and require "a positive bias applied at the gate in order to conduct current."

Ex. 1001, 1:47–54, 3:16–17. The '294 patent further explains that use of a compensated semiconductor layer 38 also "leads to low gate leakage during device operation" and "reduces the gate capacitance of the device" as compared to the prior art enhancement mode transistor discussed above. *Id.* at 3:17–21.

The '294 patent further explains that

> [t]he critical step in the above process that differentiates the device of the present invention from the prior art device (FIG. 1) is the passivation of a p-type impurity using hydrogen. The passivation leads to two differences. First, in GaN transistor 1, the compensated semiconductor layer 38 is a highly compensated semi-insulating material, while in GaN transistor 100 of the prior art, layer 105 is a conductive p-type material. Second, the capacitance of the gate electrode to channel layer is reduced in the present invention as compared to the prior art.

Ex. 1001, 3:43–52.

*D. Illustrative Claim*

Claims 1 and 7 of the '294 patent are independent. Claim 1 is representative of the challenged claims and is reproduced below.

> 1. [1p] A column III Nitride transistor comprising:
> [1a] a substrate,
> [1b] a set of III-N transition layers above the substrate,
> [1c] a III-N buffer layer above the set of transition layers,
> [1d] a III-N barrier layer above the buffer layer,
> [1e] a compensated GaN layer above the barrier layer, and
> [1f] a gate contact above the compensated GaN layer.

Ex. 1001, 5:12–18 (identifiers have been added to align with Petitioner's arguments (Pet. Claim Appendix)).

*E. Asserted Grounds of Unpatentability*

Petitioner asserts the following grounds of unpatentability (Pet. 11):

| Claims Challenged | 35 U.S.C. §[1] | Reference(s)/Basis |
|---|---|---|
| 1–12 | 103(a) | Smith[2] |
| 1–12 | 103(a) | Smith, Kigami[3] |
| 1–12 | 103(a) | Smith, Uemoto[4] |
| 1–12 | 103(a) | Uemoto, Smith |

## III. ORIGINAL CLAIMS

*A. Legal Standard*

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and "the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective

[1] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284 (2011), amended 35 U.S.C. § 103, effective March 16, 2013. Because the application from which the '294 patent issued was filed before this date, the pre-AIA version of § 103 applies.

[2] US 2007/0164315 A1, published July 19, 2007. Ex. 1005 ("Smith").

[3] JP2006-253224A, published September 21, 2006. Ex. 1008 ("Kigami") (certified translation). The original Japanese language version of Kigami is provided at Exhibit 1007.

[4] US 2008/0087915 A1, published April 17, 2008. Ex. 1006 ("Uemoto").

evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

*B. Level of Ordinary Skill in the Art*

In order to determine whether an invention would have been obvious at the time the application was filed, we consider the level of ordinary skill in the pertinent art. *Graham*, 383 U.S. at 17. In assessing the level of ordinary skill in the art, various factors may be considered, including the "type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field." *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (quotation omitted).

Petitioner contends a person of ordinary skill in the art "would have possessed at least a four-year degree in electrical engineering, chemical engineering, physics, or material science, or a closely related field, and at least two years of experience in semiconductor device design or fabrication, including the processing of semiconductor materials, analysis of device operation, or the development of new device topologies." Pet. 5–6. Petitioner contends "[a]dditional education could substitute for professional experience and vice versa." *Id.* at 6.

Patent Owner contends that a person of ordinary skill in the art would have had "at least a four-year degree in electrical engineering, physics, material science, or a closely related field, and three years of professional work experience in the epitaxial growth, design, and fabrication of

semiconductor electronic devices, including those of GaN." PO Resp. 7 (citing Ex. 2009 ¶ 82).

Upon review of the evidence of record and the parties' arguments, we adopt Petitioner's definition of the person of ordinary skill in the art as it is consistent with the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (holding that the prior art itself can reflect the appropriate level of ordinary skill in the art). We note, however, that the conclusions reached in this Decision would be the same under either proposed definition of the ordinarily skilled artisan. *See* Ex. 2009 ¶ 83 (Dr. Schubert testifying that his opinions would be the same under either proposed definition); Ex. 1033 ¶ 9 (Dr. Shealy testifying that the differences in proposed definitions of the ordinarily skilled artisan "would not change the outcome of the invalidity analysis in any material manner"); PO Resp. 7; Pet. Reply 1.

*C. Claim Construction*

In this proceeding, the claims of the '294 patent are construed "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b)." 37 C.F.R. § 42.100(b). Under that standard, the words of a claim are generally given their "ordinary and customary meaning," which is the meaning the term would have had to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

Petitioner presents a proposed construction for the term "compensated GaN layer." Pet. 12–17. Patent Owner contends the terms "compensated GaN layer" and "a gate contact above the compensated GaN layer" require

construction. PO Resp. 7–19. Patent Owner also contends that claims 1–3 should be construed to require an "enhancement-mode transistor." *Id.* at 19–23. We address the parties' claim construction disputes below.

1. *Compensated GaN layer*

Claim 1 recites "A column III Nitride transistor comprising: . . . a compensated GaN layer above the barrier layer, and a gate contact above the compensated GaN layer." Ex. 1001, 5:12–18. Petitioner contends the term "compensated" indicates that the step of compensating the GaN layer has already occurred, such that the term "compensated GaN layer" should be construed as a "'[d]oped GaN layer formed with a step to passivate its impurities' which is a 'product-by-process' limitation."[5] Pet. 12–14. And, because compensation with hydrogen was the "critical step" distinguishing the claims from the prior art, and because hydrogenation in as-grown III-nitride materials had been well known for over a decade by 2009, Petitioner contends "compensated" "cannot be interpreted as mere hydrogen presence in as-grown material, a well-known property of doped GaN." *Id.* at 15.

Patent Owner contends "compensated GaN material" should be construed as "a semiconductor GaN *gate* material in which one type of impurity (for example, donor) cancels the electrical effects of the other type of impurity (for example, acceptor)." PO Resp. 11 (citing Ex. 2009 ¶ 92) (emphasis added). Patent Owner contends this construction is consistent with the IEEE dictionary, which defines "compensated semiconductor" as

[5] Given that product-by-process steps in a device claim are not entitled to patentable weight, Petitioner contends "the prior art only need show a material with passivated impurities to show unpatentability, not the step to achieve it." Pet. 15–16.

"[a] semiconductor in which one type of impurity or imperfection (for example, donor) partially cancels the electric effects of the other type of impurity or imperfection (for example, acceptor)." PO Resp. 14 (quoting Ex. 2004). Patent Owner contends its construction is also consistent with the written description of the '294 patent, which explains that a compensated GaN material is part of the gate and includes a p-type impurity that imparts an electrical effect (i.e., conductivity), as well as a second impurity, e.g., hydrogen, that partially cancels the electrical effect of the p-type impurity, rendering the layer semi-insulating. *Id.* at 14–15 (citing Ex. 1001, 3:10–13, 3:43–45).

On this record, we construe "compensated GaN layer" as "a GaN layer in which one type of impurity (for example, donor) partially cancels the electric effects of the other type of impurity (for example, acceptor)." This is consistent with the disclosures of the '294 patent, the IEEE dictionary definition, and the construction ultimately adopted by the ITC. Ex. 2004, 3; Ex. 1049, 16–17 (ITC construing "compensated GaN layer" to mean "a GaN layer in which one type of impurity partially cancels the electrical effects of another type of impurity"); Ex. 1001, 3:43–45 (explaining that the compensated GaN layer of the '294 patent is formed through the "passivation of a p-type impurity using hydrogen"). For the reasons set forth below, however, we decline to construe "compensated GaN layer" as a product-by-process claim term (as asserted by Petitioner), or to limit the compensated GaN layer to a gate material (as asserted by Patent Owner).

2. *Whether "Compensated GaN Layer" is a Product-by-Process Limitation*

Independent claim 1 is directed to "[a] column III Nitride transistor," an apparatus. Ex. 1001, 5:12. We generally must "take care to avoid reading process limitations into an apparatus claim." *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1344 (Fed. Cir. 2008). And, when a limitation could connote either a structural characteristic of the product or a process of manufacture, we "by default" interpret that limitation in its "structural sense, unless the patentee has demonstrated otherwise." *In re Nordt Dev. Co.*, 881 F.3d 1371, 1375–76 (Fed. Cir. 2018).

The evidence of record demonstrates that a compensated GaN layer is a GaN based-layer in which the electrical effects of one impurity (structure) are partially cancelled by another impurity (structure) within the GaN layer (structure). Ex. 1001, 3:10–12 ("Compensated semiconductor layer 38 preferably comprises AlGaN or GaN with a deep level passivated p-type impurity, such as, for example, Mg, Zn, Be, Cd, or Ca."), 3:33–39 ("An additional hydrogen passivation can be performed by exposing the device to ammonia or hydrogen plasma at high temperatures."), 3:43–45 (explaining that "[t]he critical step in the above process that differentiates the device of the present invention from the prior art device (FIG. 1) is the passivation of a p-type impurity using hydrogen"); Ex. 2004, 3. This GaN layer is a structural part of the claimed "transistor," and requires specific components within its structure, e.g., magnesium dopants that interact with hydrogen to form Mg-H complexes. Ex. 1003 ¶ 63. Thus, we find that the term "compensated GaN layer" is not a product-by-process limitation, as asserted by Petitioner.

3. *Whether the Compensated GaN Layer is a Gate Material*

Claim 1 requires "a compensated GaN layer above the barrier layer, and a gate contact above the compensated GaN layer." Ex. 1001, 5:17–18. Patent Owner contends that the placement of the compensated GaN layer above the barrier layer and below the gate contact, when considered in light of the written description of the '294 patent, requires that the compensated GaN layer be part of the gate structure. PO Resp. 7–14.

When addressing the proper scope of a claim term we must look first to the intrinsic evidence of record, including the claims, written description, and prosecution history (if in the record). *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996).

*Claims*

Claim terms are generally given their ordinary and customary meaning, which is the "meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Phillips*, 415 F.3d at 1313. Patent Owner presents no evidence that the ordinary meaning in the art of a "GaN layer" is a "GaN gate material." Indeed, the prior art of record discloses multiple GaN layers that do not appear to be "gate material." Ex. 1006 ¶ 32; Ex. 1005 ¶ 74 ("the channel layer 20 is GaN"); Ex. 1008 ¶¶ 24–25 (noting that the buffer layer and the semiconductor layer are GaN). Nor does Patent Owner contend that the term "compensated" requires or implies a particular orientation or location with respect to the gate contact. Thus, by itself, the term "compensated GaN layer" does not require that it is part of the gate.

Patent Owner contends that given the placement of the "compensated GaN layer" above the barrier layer and below the gate contact, one of ordinary skill in the art would have understood that the claimed

"compensated GaN layer" "is a GaN gate material." PO Resp. 11. We are not persuaded by this argument for at least two reasons. First, the claim only requires that the compensated GaN layer is located somewhere above the barrier layer, and when the inventors intended for the compensated or semi-insulating layer to be positioned not just generally above/below other layers, but specifically between the gate contact and an underlying layer, they knew how to articulate such a configuration. For example, independent claim 10 specifically requires that the semi-insulating III-N layer is "between the barrier layer and the gate contact." Ex. 1001, 6:18–23. Second, the prior art (Uemoto) discloses a compensated GaN layer that is above a barrier layer and below a gate contact, as recited in claim 1, and Patent Owner contends this layer is not a "compensated GaN layer" because the 2DEG is present under it. Ex. 1006, Fig. 7; PO Resp. 52. This suggests that the placement of a "compensated GaN layer" above a barrier layer and below a gate contact, without more, does not indicate that the "compensated GaN layer" is part of the gate.

*Written Description*

Patent Owner notes that the '294 patent is titled "Compensated Gate MISFET and Method for Fabricating Same" and contends that "the entirety of the specification refers solely to a compensated GaN *gate* material." PO Resp. 12 (emphasis added). Patent Owner further contends that the written description indicates that the benefits of the disclosed invention are "low *gate* leakage" and "reduce[d] [] *gate* capacitance," which were achieved using a compensated material that is part of the gate. *Id.* at 12–13 (citing Ex. 1001, 1:55–2:6, 3:17–21, code (54)). According to Patent Owner, a construction of "compensated GaN layer" that does not require the layer to be part of the gate would "not meet the goals of the invention" and

would therefore be incorrect. *Id.* at 8, 12. Consistent with this understanding, Patent Owner contends that there are no disclosed embodiments in which a compensated GaN material or layer is not part of the gate structure. Sur-reply 5–6.

Although we must always interpret claim terms in light of the specification, it is the clams that define the right to exclude. *See Innova/Pure Water v. Safari Water Filtration*, 381 F.3d 1111, 1115 (Fed. Cir. 2004) ("It is a bedrock principle of patent law that the claims of a patent define the invention to which the patentee is entitled the right to exclude."); *Vitronics*, 90 F.3d at 1582 ("Thus, the specification is always highly relevant to the claim construction analysis."). Petitioner identifies no term, or combination of terms, in independent claim 1 that requires the "compensated GaN" layer be part of the gate.

As argued by Patent Owner, much of the focus of the '294 patent is on the use of a "compensated GaN" layer under a gate contact to achieve the dual goals of "low gate leakage" and reduced "gate capacitance." PO Resp. 8, 12. We may not, however, import limitations from the specification into the claims. *See Renishaw PLC v. Marposs Societa'per Azioni*, 158 F.3d 1243, 1248 (Fed. Cir. 1998) ("The difficulty is that if we once begin to include elements not mentioned in the claim in order to limit such claim . . . , we should never know where to stop.") (quoting *McCarty v. Lehigh Val R.R.*, 160 U.S. 110, 116 (1895)). This is true even if every embodiment in the patent places the compensated GaN layer directly under the gate, as asserted by Patent Owner. *See Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1366 (Fed. Cir. 2012) ("It is likewise not enough that the only embodiments, or all of the embodiments, contain a particular

limitation. We do not read limitations from the specification into claims; we do not redefine words.").

There are two exceptions to the general rule that we apply the ordinary and customary meaning of a claim term: (1) when a patentee sets out a definition and acts as his own lexicographer, or (2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution. *See Thorner*, 669 F.3d at 1365. The standards for lexicography and disclaimer, however, are "exacting." *Id.* at 1366.

There is no argument that the patentees acted as their own lexicographer to redefine the term "compensated GaN layer." With respect to disavowal, a "patentee may demonstrate intent to deviate from the ordinary and accustomed meaning of a claim term by including in the specification expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope." *Thorner*, 669 F.3d at 1366 (quoting *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1325 (Fed. Cir. 2002)). As noted by Patent Owner, the title of the '294 patent is, in part, "Compensated Gate MISFET" and much of the discussion of the '294 patent is of a compensated GaN layer that is directly below the gate contact and above a barrier layer and operates in conjunction with the gate contact to control the on/off state of the transistor. PO Resp. 12–14. We are presented with insufficient argument or evidence to conclude, however, that these disclosures rise to the level of a disclaimer. For example, although the title of the '294 patent is directed to a "Compensated Gate MISFET," claim 1 is more broadly directed to "[a] column III Nitride transistor." Ex. 1001, 5:12, code (54). Nor are we directed to an expression or statement of manifest exclusion in the '294 patent that would serve to disclaim any "compensated GaN layer" that is not directly below the gate and/or that does not function

in concert with the gate electrode to control the on/off state of the transistor. *See Thorner*, 669 F.3d at 1366.

With respect to the stated goals of the invention, as noted by Patent Owner, one of the primary purposes of the compensated GaN layer of the '294 patent is to reduce gate leakage and gate capacitance. Ex. 1001, 2:13–19, 3:18–21 ("[U]sing a compensated semiconductor layer 38 leads to low gate leakage during device operation."). We cannot use the goals of the invention, however, to rewrite the claims or insert terms that are not present. *See Thorner*, 669 F.3d at 1366. Moreover, the prior art of record indicates that a compensated GaN layer that is below the gate contact and above a barrier layer, but not part of the active gate structure, may also "decrease the leakage current between the gate and the drain." Ex. 1006 ¶¶ 44 ("Even when a positive bias of 5 V or higher is applied to the gate electrode, no significant gate-leakage current is observed."), 61. As such, evidence of record suggests that a person of ordinary skill in the art would have understood that one of the primary goals disclosed in the '294 patent is achieved regardless of whether the compensated GaN layer is part of the gate, or simply in close vicinity to the gate.

In view of the foregoing, we are not persuaded that the written description of the '294 patent indicates that the "compensated GaN layer" must be part of the gate structure.

*Prosecution History*

Neither party asserts that the prosecution history provides helpful guidance on the question of whether a "compensated GaN layer" requires this layer to be part of the gate. *See generally* Pet. 13–17; PO Resp. 7–19.

*Conclusion*

In view of the foregoing, we determine that the intrinsic evidence of record does not support construing "compensated GaN layer" as a "compensated GaN gate material." As such, we construe "compensated GaN layer," consistent with the ITC's construction, as "a GaN layer in which one type of impurity (for example, donor) partially cancels the electric effects of the other type of impurity (for example, acceptor)."

4. *Whether Claims 1–3 are Directed to an Enhancement Mode Transistor*

Patent Owner contends that if a p-doped, compensated GaN layer is used under a gate electrode, as depicted in the '294 patent, then the transistor will be an enhancement mode device. PO Resp. 19–23. Thus, Patent Owner contends claims 1–3 are directed to an enhancement mode transistor. *Id.* As a predicate to this argument, however, the claimed "compensated GaN layer" must be directly under the gate contact, or otherwise be part of the gate. *Id.* at 21. As discussed above, we do not construe "compensated GaN layer" to require a "compensated GaN gate material." As such, we are not persuaded that claims 1–3 are limited to an enhancement mode transistor.

*D. Statement of Disputed Facts*

Pursuant to 37 C.F.R. § 42.22(c), a petition "may include a statement of material facts." "Each material fact preferably shall be set forth as a separately numbered sentence with specific citations to the portions of the record that support that fact." *Id.*

Petitioner provides 13 statements of material fact regarding "the state of III-nitride transistor technology at the time of the '294 patent['s] claimed

priority date." Pet. 11–13. Petitioner does not, however, provide specific citations to the portions of the record that support these material facts. *Id.*

Patent Owner contends Petitioner's statement of material facts "is materially deficient and should be ignored" because "Petitioner failed to include any citations to the record supporting any of its alleged facts." PO Resp. 23.

Petitioner's failure to provide citations supporting its statements of material fact is highly problematic. It essentially shifts the burden of proving the facts are incorrect to Patent Owner, without Petitioner having to provide citations to support its assertions. We need not determine whether such an omission requires ignoring the statements of material fact in this case, however, because the recited material facts are either clearly supported by the evidence of record or not necessary to render a Decision in this case.

*E. Secondary Considerations of Non-Obviousness*

Objective indicia of non-obviousness, or secondary considerations of non-obviousness, serve "an important role as a guard against the statutorily proscribed hindsight reasoning in the obviousness analysis," and must be considered in every case in which they are presented. *WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1328 (Fed. Cir. 2016). Objective indicia may include evidence of a long-felt need in the art, praise within the industry, skepticism in the industry about whether or how a problem could be solved, copying, and commercial success. *Id.* at 1132–37.

To be probative, Patent Owner must prove there is a nexus between the presented evidence and the merits of the claimed invention. *See Demaco Corp. v. F. Von Langsdorff Licensing Ltd.*, 851 F.2d 1387, 1392 (Fed. Cir. 1988). A rebuttable presumption of nexus applies when the "patentee shows

that the asserted evidence is tied to a specific product and that the product '*is* the invention disclosed and claimed.'" *Fox Factory, Inc. v. SRAM, LLC*, 944 F.3d 1366, 1373 (Fed. Cir. 2019) (quoting *Demaco*, 851 F.2d at 1392). "That is, presuming nexus is appropriate 'when the patentee shows that the asserted objective evidence is tied to a specific product and that product embodies the claimed features, and is coextensive with them.'" *Id.* (quoting *Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1072 (Fed. Cir. 2018)). If the praise is not limited to the features of the claimed invention, the patent owner may still prove nexus "by showing that the evidence of secondary considerations is the 'direct result of the unique characteristics of the claimed invention.'" *Id.* at 1373–74 (quoting *In re Huang*, 100 F.3d 135, 140 (Fed. Cir. 1996)).

Patent Owner contends that the compensated gate of the '294 patent "was a breakthrough invention and resulted in the first commercially viable enhancement-mode GaN transistor." PO Resp. 60 (citing Ex. 2009 ¶¶ 192–193, 197; Ex. 2021). Patent Owner further contends that this achievement required the counter-intuitive use of a compensated gate material in the gate structure, and represented "a technological leap that laid the foundation for viable enhancement-mode GaN transistors." *Id.* at 61–62. For this achievement, Patent Owner contends the inventor, Dr. Alex Lidow, received the 2015 SEMI Award. *Id.* at 60 (citing Ex. 2021).

Upon review of Patent Owner's evidence and the parties' arguments, we find that Patent Owner's objective indicia evidence is entitled to little, if any, weight. The evidence of praise relied upon by Patent Owner is not clearly linked to the claimed invention or any particular product having each of the claimed features of the '294 patent. Ex. 2021. For example, the 2015 SEMI award was provided to Dr. Lidow "for commercialization of GaN

power devices." *Id.* An article explaining the award indicates that "high cost" previously "limited [the] commercial success" of GaN technologies, but Dr. Lidow was able to overcome these issues, "from resolving packaging limitations to establishing a low-cost supply chain," "through persistence." *Id.* This praise is not demonstrably linked to the claimed invention or any particular device, and does not mention the use of a compensated gate, or any other relevant feature recited in the claims.

In view of the foregoing, we determine that Patent Owner's objective evidence of non-obviousness is entitled to little, if any, weight.

*F. Claims 1–3 and 7–9 over Uemoto and Smith*

Petitioner contends that the subject matter of claims 1–3 and 7–9 would have been obvious over the combined disclosures of Uemoto and Smith.[6] Pet. 61–77, 80–82.

1. *Uemoto*

Uemoto is titled "Nitride Semiconductor Device and Method for Fabricating the Same" and published April 17, 2008. Ex. 1006, codes (43), (54). The nitride semiconductor device of Uemoto

> is characterized in that it includes: a first nitride semiconductor layer; a second nitride semiconductor layer; a third nitride semiconductor; and a gate electrode. The first nitride semiconductor layer is formed over a substrate. The second nitride semiconductor layer is formed on the first nitride semiconductor layer and has a wider band gap than the first nitride semiconductor layer. The third nitride semiconductor

[6] As discussed above, although the Petition challenges claims 1–12, Patent Owner filed a non-contingent Motion to Amend requesting to cancel claims 4–6 and 10–12. Mot. 1–2. We grant the Motion to Amend in that respect and, thus, only claims 1–3 and 7–9 remain in this proceeding. *See infra* Section IV.

> layer is formed on the second nitride semiconductor layer and includes a control region with a p-type conductivity and a high resistive region formed around the control region and having a higher resistance than that of the control region. The gate electrode is formed on the control region.

*Id.* ¶ 13. According to Uemoto, the disclosed semiconductor device "has a large operating current with normally-off operation and excellent switching characteristics." *Id.* ¶ 11.

Figure 7 of Uemoto is reproduced below.

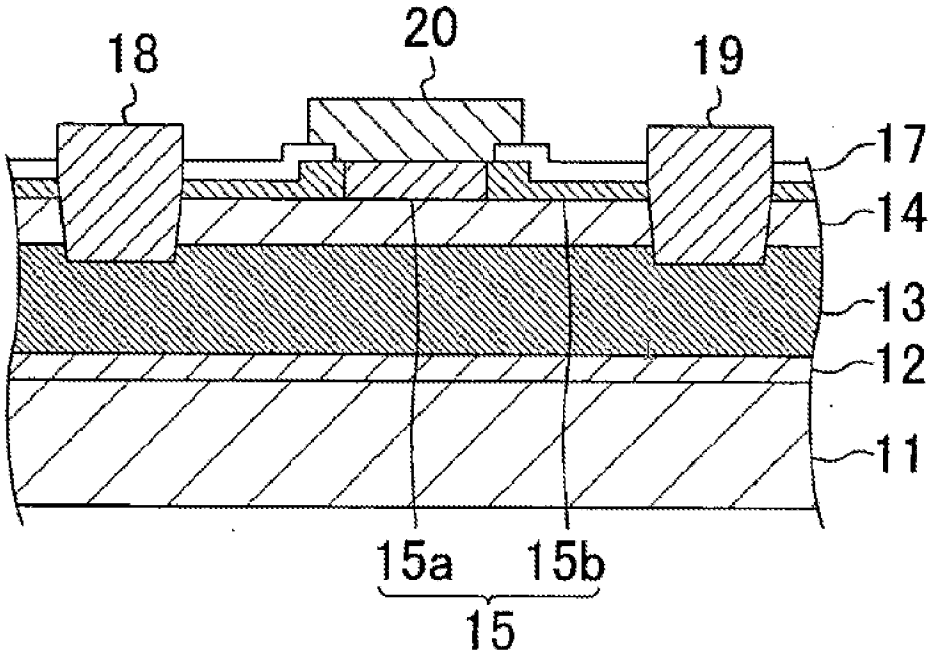



Figure 7 of Uemoto is "a cross sectional view showing a nitride semiconductor transistor according to a third embodiment" of Uemoto. Ex. 1006 ¶ 23. The transistor depicted in Figure 7 is composed of substrate 11, buffer layer 12, first nitride semiconductor layer 13, second nitride semiconductor layer 14, third nitride semiconductor layer 15, hydrogen diffusion film 17, source electrode 18, drain electrode 19, and gate electrode 20. *Id.* ¶¶ 31–35, 57, 62–63.

Uemoto explains that the third nitride semiconductor layer 15 is doped with Mg. Ex. 1006 ¶¶ 33, 46. Hydrogen diffusion film 17 is made of silicon nitride (SiN) and contains at least $1x10^{20}/cm^3$ hydrogen. *Id.* ¶ 63. During thermal treatment, hydrogen from hydrogen diffusion film 17 selectively inactivates the impurities in region 15b, whereas impurities in control region 15a, which is not covered by hydrogen diffusion film 17, are activated to selectively form a region having p-type conductivity. *Id.* According to Uemoto, the high resistance of region 15b reduces the leakage current between the gate and the drain. *Id.* ¶ 59.

2. *Smith*

Smith discloses transistors that incorporate nitride-based active layers. Ex. 1005 ¶ 2. Smith explains that silicon (Si) and gallium arsenide (GaAs) have found wide application in low power semiconductor devices, but are not well suited for higher power and/or high frequency applications due to their relatively small bandgaps (e.g., 1.12 eV for Si and 1.42 for GaAs at room temperature) and/or relatively small breakdown voltages. *Id* ¶ 3. In light of these difficulties, interest in high power, high temperature, and/or high frequency applications has turned to semiconductors with wide bandgaps, such as silicon carbide and Group III nitrides. *Id.* ¶ 4.

One application of these materials is in a HEMT, which may offer operational advantages due to the formation of a two-dimensional electron gas (2DEG) at the heterojunction of two semiconductor materials with different bandgap energies, and where the smaller bandgap material has a higher electron affinity. Ex. 1005 ¶ 5.

Figure 2A of Smith is reproduced below.

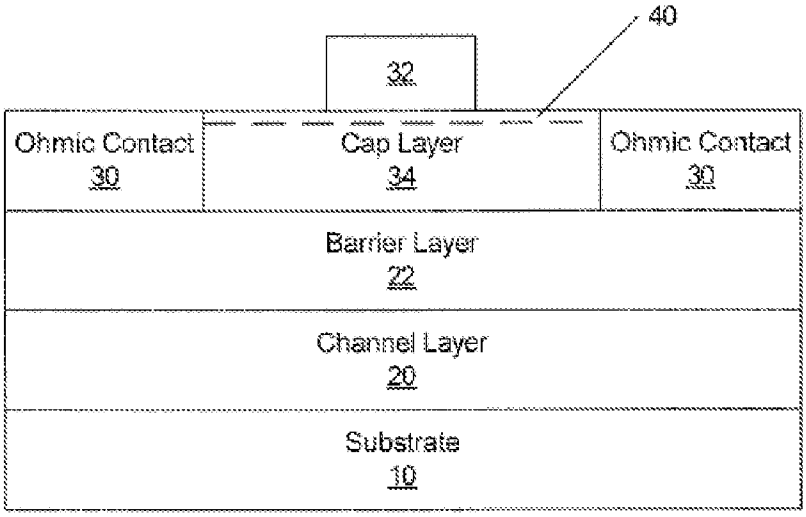



Figure 2A

Figure 2A is a cross-sectional schematic illustrating transistors having a cap layer. Ex. 1005 ¶ 41. In the embodiment schematically depicted in Figure 2A, substrate 10 may be a semi-insulating silicon carbide layer. *Id.* ¶ 69. "Optional buffer, nucleation and/or transition layers (not shown) may be provided on the substrate 10." *Id.* ¶ 70. Channel layer 20 is formed above substrate 10 and barrier layer 22 is formed above channel layer 20. *Id.* ¶¶ 73, 85. Channel layer 20 may be composed of $Al_xGa_{1-x}N$ where $0 \leq x < 1$ (which allows for GaN when x=0). *Id.* ¶ 74. Barrier layer 22 is composed of AlN, AlInN, AlGaN, or AlInGaN and has a smaller electron affinity and greater bandgap than channel layer 20. *Id.* ¶ 75. Cap layer 34 may be a GaN layer and includes a doped region 40 at or near its outer surface. *Id.* ¶ 85. Cap layer 34 may be blanket formed on barrier layer 22 and may be epitaxially grown and/or formed by deposition. *Id.* ¶ 77. Doped region 40 may be doped with a p-type dopant, such as Mg, Be, Zn, Ca and/or C. *Id.* ¶¶ 85, 87. In another embodiment, doped region 40 is doped with deep level

dopants, such as Fe, C, V, Cr, Mn, Ni, Co or other rare earth elements. Ex. 1005 ¶ 89.

Smith explains that the p-type and deep level dopants in these embodiments "may be used to screen the channel region from surface states, [and] pin the surface energy level at a predictable and desired level to reduce and/or minimize trapping effects and to reduce leakage currents." *Id.* ¶¶ 87, 89. Smith further explains that "[t]he level of doping should be sufficiently high so as to reduce leakage current in embodiments without a recessed gate and be the dominant 'surface' state but no so high as to provide introduce [sic] traps or leakage paths by becoming a conductive layer" (p-type dopant embodiment) or "so high as to cause significant trapping" (deep level dopant embodiment). *Id.*

3. *Analysis—Claim 1*

Petitioner contends that Uemoto and Smith teach or suggest every limitation of independent claim 1. Pet. 61–76. In particular, Petitioner contends that Uemoto discloses a "nitride semiconductor transistor[]" (element [1p]) that includes a substrate 11 (element [1a]), a buffer layer 12 (identified as "transition layers" by Petitioner) that is above substrate 11 (element [1b]), a first nitride semiconductor layer 13 that is a buffer layer and is above the transition layers (buffer layer 12) (element [1c]), a second nitride semiconductor layer 14 that is a barrier layer and is above the buffer layer (element [1d]), a compensated GaN layer 15b that is above the barrier layer (element [1e]), and a gate electrode 20 that is above the compensated GaN layer (element [1f]). *Id.* at 68–76. Although buffer layer 12 is depicted as a single layer and not as "a set of transition layers," Petitioner contends that one of ordinary skill in the art would have sought to use a set of

transition layers in Uemoto to achieve "strain balancing" and lower gate leakage, as taught in Smith. *Id.* at 62–64, 69–70. With respect to the requirement that the gate contact is above the compensated GaN layer, Petitioner contends that Figure 7 of Uemoto depicts gate electrode 20 above, or higher than, region 15b, as well as portions of region 15b that are directly below and in direct contact with gate electrode 20. *Id.* at 75; *see id.* at 74–75 n.5 (providing district court decisions construing "above" as "higher than, but not necessarily in contact with," "over," or "in a higher place than or overhead").

Patent Owner contends Uemoto and Smith do not render independent claim 1 obvious because (a) the "compensated GaN layer" of Uemoto has no 2DEG beneath it; and (b) Uemoto's gate electrode is not located above the alleged compensated GaN layer. PO Resp. 50–58. We address these arguments below.

a. *No 2DEG Below the Compensated GaN layer*

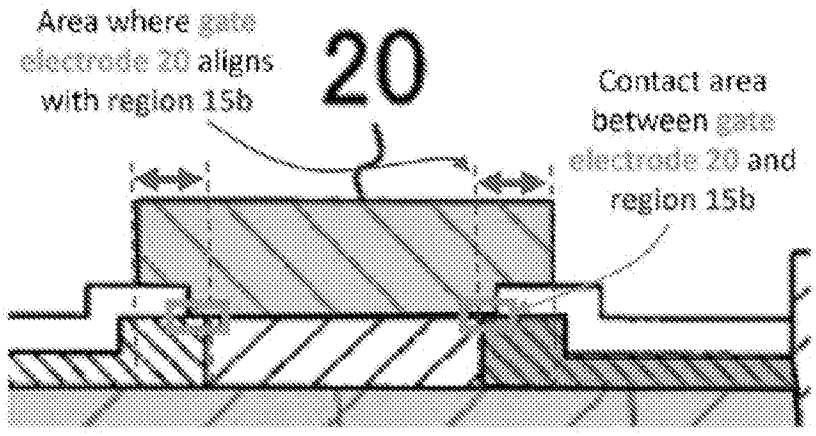
Patent Owner contends it is undisputed that the area under the "compensated GaN layer" of Uemoto (region 15b) has a 2DEG below it at zero volts applied gate bias. PO Resp. 50–51. As such, Patent Owner contends region 15b of Uemoto "cannot correspond to the compensated GaN layer of claim 1." *Id.* at 52.

This argument is not persuasive because, as noted by Petitioner, claim 1 does not require an enhancement mode device or the absence of a 2DEG region below either the gate or the compensated GaN layer at zero volts applied gate bias. Ex. 1001, 5:12–18; Pet. Reply 22–23.

b. *Gate Contact Above the Compensated GaN Layer*

Patent Owner contends region 15b of Uemoto "cannot correspond to the compensated GaN layer because the design of *Uemoto* precludes its device from providing both the reduced gate leakage current and reduced gate capacitance that the '294 Patent's transistor offers over the prior art." PO Resp. 56. And, although Figure 7 is depicted with a small portion of region 15b directly under the gate contact, Patent Owner contends it is activated region 15a that is below the gate and part of the gate structure. *Id.* at 57. Patent Owner further argues that there is no narrative disclosure in Uemoto of layer 15b being below the gate electrode, and the pictorial support of "layer" 15b being below the gate is lacking because the "sliver" that Petitioner is referring to "is not a layer (as required by claim 1 of the '294 patent)." *Id.* at 58.

Petitioner argues in its Reply that the claims merely require that the "gate contact" be "above" the compensated GaN layer and "*Uemoto* plainly discloses its gate electrode is 'above' region 15b," which is a "compensated GaN layer." Pet. Reply 23. In support of its arguments, Petitioner provides the following annotated and enlarged version of Figure 7 of Uemoto.




*Uemoto*, Fig. 7 (annotated)

Figure 7 above is annotated to show the region where Petitioner contends gate electrode 20 of Uemoto aligns with and/or contacts region 15b. Petitioner contends that Figure 7 discloses electrode 20 "above" region 15b and, at least partially, directly on top and in contact with region 15b. *Id.* at 24. And, even though Uemoto's text does not describe the gate as being in contact with region 15b, Petitioner contends Figure 7 clearly shows this configuration and features of drawings need not be described in the specification to be prior art. *Id.* at 25 (citing MPEP § 2125; *In re Aslanian*, 590 F.2d 911, 914 (CCPA 1979)).

Upon review of the parties' arguments and supporting evidence, and in particular Figure 7 of Uemoto, we find Petitioner's argument persuasive that Uemoto teaches or suggests a gate contact that is above a "compensated GaN layer." First, Petitioner persuasively demonstrates that region 15b of Uemoto is a GaN *layer* that has its p-type dopants compensated by hydrogen. Pet. 72–73 (citing Ex. 1006 ¶¶ 33, 49, 54, 63 (noting that element 15 is a "layer")). Second, Petitioner persuasively demonstrates that gate electrode 20 is at all locations "above," or higher than, compensated GaN

layer 15b, as well as in contact with the top surface of this layer in at least two locations along its periphery. Pet. 73–74; Pet. Reply 23–24.

Patent Owner's arguments to the contrary are not persuasive. As discussed above, the claims do not require that the compensated GaN layer be part of the gate structure, or reduce gate leakage or capacitance. Nor do the claims require that any part of, much less the entire, compensated GaN layer be directly below the gate or operate in conjunction with the gate contact to control the on/off state of the transistor.

In view of the foregoing, Petitioner persuasively demonstrates that Uemoto and Smith teach or suggest every limitation of claim 1. Petitioner also provides a persuasive, uncontested explanation as to why one of ordinary skill in the art would have used the transition layers of Smith in Uemoto. Pet. 66–67, 69–70 (explaining that Smith's transition layers would provide "strain balancing," would "reduce or prevent alloy scattering," and would serve to keep "gate leakage low" and improve electron mobility). Accordingly, Petitioner demonstrates by a preponderance of the evidence that claim 1 would have been obvious over Uemoto and Smith.

4. *Claim 7*

Independent claim 7 is similar to independent claim 1, but requires "a semi-insulating III-N layer above the barrier layer, and a confinement layer above the semi-insulating III-N layer."[7] Ex. 1001, 6:6–12; Pet. 81.

With respect to elements [7a]–[7e], Petitioner's identifications of where these claim elements are found in Uemoto and Smith are identical to

[7] In contrast to independent claim 1, independent claim 7 does not require a gate contact above the semi-insulating III-N layer (or the confinement layer). *Id.*

those for elements [1a]–[1c] and [4d][8]. Pet. 80. With respect to element [7f] ("confinement layer above the semi-insulating III-N layer"), Petitioner contends that Uemoto discloses a hydrogen diffusion layer 17 that is on top of the third nitride semiconductor layer 15 and is "made of silicon nitride," which is the same material that the '294 patent associates with the "confinement layer." *Id.* at 80–82 (citing Ex. 1001, 4:34–35; Ex. 1006 ¶ 63; Ex. 1003 ¶¶ 272–74).

With respect to element [7e], Petitioner contends that one of ordinary skill in the art would have sought to make nitride semiconductor layer 15 in Uemoto semi-insulating in view of the disclosures of Smith. Pet. 64, 78, 80–81. In particular, Petitioner contends that Smith discloses doping with deep level dopants to form a semi-insulating layer and Saxler,[9] incorporated by reference in Smith, discloses using co-doping to create a semi-insulating nitride layer. *Id.* (citing Ex. 1005 ¶¶ 85, 89; Ex. 1016 ¶¶ 18–19, 27, Fig. 3; Ex. 1003 ¶ 225).

Petitioner contends one of ordinary skill in the art would have understood that using Smith's semi-insulating layer in Uemoto would be advantageous because it would further Uemoto's goals of reduced leakage current, improved device fabrication, and improved transistor stability. Pet. 64–65. Petitioner further contends that substitution of Uemoto's p-type magnesium doping with the deep level dopants of Smith or Smith's method of co-doping would have been a simple substitution of known doping elements or techniques to achieve predictable results. *Id.* at 66.

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[8] Elements [4d] and [7d] require a "III-N barrier layer." There is no dispute that Uemoto discloses this element. Pet. 71, 78, 80.

[9] US Pub. No. 2005/0145874 A1 (Ex. 1016, "Saxler").

Patent Owner contends Petitioner's arguments with respect to independent claim 7 suffer from a critical flaw—Smith never discloses a semi-insulating cap layer or using Saxler's co-doping with a shallow level p-type dopant and a deep level dopant. PO Resp. 58–60. According to Patent Owner, Smith only discloses utilizing different *concentrations* of dopants throughout the cap layer. *Id.* at 60.

Smith discloses that cap layer 34 may be a GaN layer and may include a doped region 40 at or near its outer surface. Ex. 1005 ¶ 85. Doped region 40 may be doped with a p-type dopant, such as Mg, Be, Zn, Ca and/or C. *Id.* ¶¶ 85, 87. The "[p]-type dopants may be used to screen the channel region from surface states, [and] pin the surface energy level at a predictable and desired level to reduce and/or minimize trapping effects and to reduce leakage currents." *Id.* ¶ 87. Smith goes on to disclose that region 40 may also be doped with an n-type dopant or a deep level dopant. Ex. 1005 ¶ 85. "In some embodiments . . . the cap layer 34 has a dopant incorporated throughout the cap layer 34, 34'. In such a case, the doped region 40 may be provided by a region of increased dopant concentration over the concentration of dopant in the remainder of the cap layer 34, 34'." *Id.* Immediately after this disclosure, and in the same paragraph, Smith states:

> Techniques for co-doping Group III-nitride materials are described, for example, in U.S. patent application Ser. No. 10/752,970, filed Jan. 7, 2004 entitled "CO-DOPING FOR FERMI LEVEL CONTROL IN SEMI-INSULATING GROUP III NITRIDES," the disclosure of which is incorporated herein as if set forth in its entirety.

*Id.* The application incorporated by reference is Saxler, which discloses co-doping a nitride layer with a shallow level p-type dopant and a deep level

dopant, such as Fe, Co, Mn, Cr, V and/or Ni, to form a semi-insulating layer. Ex. 1016 ¶¶ 5–6, Claim 1, code (57).

We agree with Petitioner that Smith's incorporation-by-reference of Saxler in its entirety, and in particular its techniques for co-doping group III nitrides to form semi-insulating layers (provided within a paragraph discussing the doping of cap layer 34), serves to expressly teach or suggest co-doping cap layer 34 of Smith to form a semi-insulating group III-N layer. Pet. 64–65, 81; Pet. Reply 25–26; *Paice LLC v. Ford Motor Co.*, 881 F.3d 894, 906 (Fed. Cir. 2018); *Advanced Display Sys., Inc. v. Kent State Univ.*, 212 F.3d 1272, 1282 (Fed. Cir. 2000) ("Incorporation by reference provides a method for integrating material from various documents into a host document . . . by citing such material in a manner that makes clear that the material is effectively part of the host document as if it were explicitly contained therein."). Accordingly, Petitioner persuasively identifies where Uemoto and Smith teach or suggest every limitation of independent claim 7. Petitioner also persuasively explains why one of ordinary skill in the art would have sought to combine the two disclosures to arrive at the subject matter of claim 7 with a reasonable expectation of success. Pet. 64–65 (asserting that the proposed combination would reduce leakage current and improve device fabrication), 81. Thus, Petitioner demonstrates by a preponderance of the evidence that the subject matter of claim 7 would have been obvious in view of Uemoto and Smith.

5. *Claims 2 and 3*

Claim 2 depends from claim 1 and further requires that the compensated GaN layer "contains acceptor type dopant atoms passivated with hydrogen." Ex. 1001, 5:19–21. Claim 3 depends from claim 2 and

further requires "where the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca." *Id.* at 5:22–23.

Petitioner contends that the combination of Uemoto and Smith discloses the subject matter of claims 2 and 3 because layer 15 of Uemoto is doped with magnesium, which is a p-type (acceptor-type) dopant, and this magnesium is passivated by hydrogen. Pet. 76–77 (citing Ex. 1006 ¶¶ 33, 46, 63).

Patent Owner contends Uemoto does not disclose all of the elements of claims 2 and 3. PO Resp. 53. Patent Owner reasons that claims 2 and 3 are directed to an enhancement mode device and, because "an enhancement-mode transistor is normally OFF due to a depleted 2DEG at zero voltage, it follows that the enhancement-mode transistor recited by claims 2 and 3 has no 2DEG below the hydrogen-passivated p-GaN at zero voltage." *Id.* at 52–54 (citing Ex. 2015, 442:17–443:18; Ex. 2016, 934:2–3; Ex. 2009 ¶ 175). In contrast, Patent Owner contends Uemoto's highly resistive region 15b has an intact 2DEG below it and, therefore, "cannot correspond to the hydrogen-passivated p-GaN recited in claims 2 and 3." *Id.* at 54–55 (citing Ex. 2009 ¶ 176).

Patent Owner's arguments are not persuasive for at least two reasons. First, we do not construe claims 2 and 3 to require an enhancement mode device. Second, even if an enhancement mode device were required, there is no dispute that Uemoto's device is an enhancement mode device, and Patent Owner identifies no limitation in claims 2 or 3 that would require that the "compensated GaN layer" cause the depletion of the 2DEG layer under the gate contact. Ex. 2009 ¶¶ 170–171 (Dr. Schubert testifying that the 2DEG is depleted under the activated region 15a of Uemoto); Ex. 1006 ¶ 11 (Uemoto explaining that the "present invention" provides a semiconductor device

"which has a large operating current with normally-off operation");
Pet. Reply 22.

In view of the foregoing, Petitioner persuasively identifies where every limitation of claims 2 and 3 is disclosed in Uemoto and Smith. Petitioner also persuasively explains why one of ordinary skill in the art would have sought to combine Uemoto and Smith to arrive at the subject matter recited in claims 2 and 3 with a reasonable expectation of success. Accordingly, Petitioner demonstrates by a preponderance of the evidence that claims 2 and 3 would have been obvious over Uemoto and Smith.

6. *Claims 8 and 9*

Claim 8 depends from claim 7 and further requires "wherein the semi-insulating III-N layer contains deep acceptor type dopant atoms selected from the group consisting of C, Fe, Mn, Cr, and V." Ex. 1001, 6:13–15. Claim 9 depends from claim 7 and further requires "wherein the confinement layer is made of SiN, $SiO_2$, $Al_2O_3$, $HfO_2$, $Ga_2O_3$, or InAlGaN." *Id.* at 6:16–17.

Petitioner identifies where Uemoto and Smith teach or suggest every limitation of claims 8 and 9, including the use of deep acceptor type dopants ("the deep level dopants may be Fe, C, V, Cr, Mn, Ni, Co or other rare earth elements") and a SiN confinement layer. Pet. 79–80, 82.

Patent Owner does not contest Petitioner's arguments with respect to these claims, apart from its arguments with respect to independent claim 7 discussed above. *See generally* PO Resp.

Upon review of Petitioner's arguments and supporting evidence, we determine that Petitioner demonstrates by a preponderance of the evidence

that the subject matter of claims 8 and 9 would have been obvious in view of the combined disclosures of Uemoto and Smith.

7. *Conclusion*

For the reasons set forth above, Petitioner demonstrates by a preponderance of the evidence that the subject matter of claims 1–3 and 7–9 would have been obvious in view of Uemoto and Smith.

*G. Claims 1–3 and 7–9 over Smith, Smith and Kigami, and Smith and Uemoto*

Petitioner contends the subject matter of claims 1–3 and 7–9 would have been obvious in view of Smith, Smith and Kigami, and Smith and Uemoto. Pet. 17–53. Having determined that claims 1–3 and 7–9 would have been obvious over Uemoto and Smith, we do not address Petitioner's additional grounds with respect to these claims. *See SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1359 (2018) (holding that a petitioner "is entitled to a final written decision addressing all of the claims it has challenged").

## IV. MOTION TO AMEND

Patent Owner filed a Motion to Amend the claims of the '294 patent, in which it requests cancellation of claims 4–6 and 10–12 and entry of proposed substitute claims 13 and 14, which replace claims 4 and 10, respectively. Mot. 1.

*A. Proposed Substitute Claims*

Proposed substitute claims 13 and 14 are reproduced below (underlining indicates additions and bracketing indicates deletions from each respective original claim).

13. <u>An enhancement mode</u> [A] column III Nitride transistor comprising:

a substrate,

a set of III-N transition layers above the substrate,

a III-N buffer layer above the set of transition layers,

a III-N barrier layer above the buffer layer, [and]

a semi-insulating III-N layer above the barrier layer,

wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen, and

a gate comprising a gate contact and the compensated GaN layer, wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias.

Mot. Appendix A, 1.

14. A compensated gate enhancement mode MISFET transistor comprising:

a III-N barrier layer beneath a gate contact,

a drain contact,

a source contact, and

a semi-insulating III-N layer between the barrier layer and the gate contact,

wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen, and a gate comprising the gate contact and the compensated GaN layer, wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias.

*Id.* at 1–2.

*B. Statutory and Regulatory Requirements*

"Before considering the patentability of any substitute claims, . . . the Board first must determine whether the motion to amend meets the statutory and regulatory requirements set forth in 35 U.S.C. § 316(d) and 37 C.F.R.

§ 42.121." *Lectrosonics, Inc. v. Zaxcom, Inc.*, IPR2018-01129, Paper 15 at 4 (PTAB Feb. 25, 2019) (precedential). These statutory requirements include (1) proposing a reasonable number of substitute claims per challenged claim; (2) ensuring that the motion to amend responds to a ground of unpatentability involved in the trial; (3) not enlarging the scope of the claims of the challenged patent or introducing new subject matter; and (4) providing a claim listing reproducing each proposed substitute claim. *Id.* at 4–8.

1. *Reasonable Number of Substitute Claims*

Patent Owner seeks to cancel six claims and enter two proposed substitute claims in place of cancelled claims 4 and 10. Mot. 2. This is a presumptively reasonable number of substitute claims for each cancelled claim, and Petitioner does not argue otherwise. *See Lectrosonics*, Paper 15 at 4 ("There is a rebuttable presumption that a reasonable number of substitute claims per challenged claim is one (1) substitute claim."); *see generally* Opp.

2. *Respond to a Ground of Unpatentability*

In its proposed substitute claims, Patent Owner provides additional limitations that it contends further distinguish the proposed substitute claims from the prior art asserted in the instituted grounds. Mot. 2. We agree that Patent Owner's substitute claims respond to a ground of unpatentability involved in the trial, and Petitioner does not assert otherwise.

3. *Do the Amendments Enlarge the Scope of the Claims of the Challenged Patent or Introduce New Matter?*

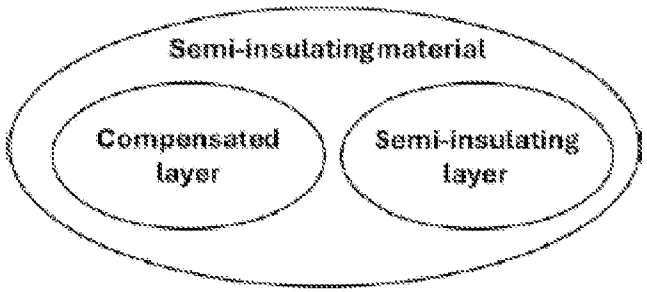
Patent Owner contends that the proposed amended claims "further limit the scope of independent claims 4 and 10" and do not add new matter. Mot. 3–7. Patent Owner provides specific citations to the '294 patent's non-

provisional application to demonstrate written description support for the challenged claims and to demonstrate that no new matter has been introduced in the proposed substitute claims. *Id.* at 4–7.

Petitioner argues that the limitation "wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen" lacks written description support and constitutes broadening new matter, because the '294 patent does not describe a "semi-insulating III-N layer" that "comprises a compensated GaN layer." Opp. 2–3. Rather, according to Petitioner, the '294 patent describes the "compensated GaN layer" and the "semi-insulating layer" as being different layers, made via different methods and used in different embodiments. *Id.* at 3 ("The patent never describes embodiments with a semi-insulating layer ***comprising*** a compensated GaN layer."), 3 (asserting that the field of invention states that "the invention relates to an enhancement mode GaN transistor with a compensated GaN layer ***or*** a semi-insulating GaN layer"), 7–8 (asserting that the proposed substitute claims "impermissibly broaden" the claims "for the same reasons they lack written description support").

Petitioner's argument is not persuasive because the '294 patent describes its "compensated semiconductor layer 38" as being "a highly compensated semi-insulating material." Ex. 1001, 3:45–49. As Dr. Schubert persuasively testifies, a GaN layer that is formed entirely of a semi-insulating material will be a semi-insulating layer and, if that layer achieves its semi-insulating state through compensation, it will be a semi-insulating compensated GaN layer. Ex. 2024 ¶ 16; Ex. 1001, 3:19–21 ("[T]he insulating nature of compensated layer 38 reduces the gate capacitance of the device."), 3:45–49; Mot. Reply 3.

Petitioner contends there is no conflict in its arguments because although both layers are made of a semi-insulating material, a "compensated layer" is not a "semi-insulating layer." Mot. Sur-reply 1. To illustrate its argument, Petitioner provides the following diagram:




In the diagram above, the ovals for the "Compensated layer" and "Semi-insulating layer" are distinct and do not overlap, but both are fully subsumed within a larger oval identified as a "Semi-insulating material." *Id.* Although the '294 patent discusses the "semi-insulating" and "compensated" semi-conductors separately, it does not clearly support Petitioner's bright line distinctions between a semi-insulating and compensated layer. Ex. 1001, 3:46–52. Rather, the evidence of record indicates that a compensated layer is a species within the broader genus of semi-insulating layers. In particular, both the compensated and semi-insulating layers may be formed of a semi-insulating material and have the electrical property of being semi-insulating, but the compensated GaN layer achieves this electrical property in a specific way, i.e., one type of impurity partially cancels the electric effects of the other type of impurity. Ex. 2004, 3; Ex. 1049, 16–17; Ex. 1001, 3:43–46; Ex. 2024 ¶ 11–18. In contrast, the claimed semi-insulating layer may achieve the electrical property of being semi-insulating in many possible ways that do not necessarily include passivation with hydrogen or another impurity. For example, the semi-

insulating layer may be obtained through the use of deep level impurity atoms, such as C, Fe, Mn, Cr, V, or Ni. Ex. 2024 ¶ 17; Ex. 1001, 3:57–59.

In view of the foregoing, we credit the testimony of Dr. Schubert and determine that Patent Owner demonstrates that the proposed substitute claims do not enlarge the scope of the claims and do not add new matter. Ex. 2024 ¶¶ 16–18.

4. *Claims Listing*

Patent Owner provides a claims listing reproducing each proposed substitute claim. Mot. Appendix A.

5. *Conclusion*

For the reasons set forth above, we determine that Patent Owner's Motion to Amend meets the statutory and regulatory requirements set forth in 35 U.S.C. § 316(d) and 37 C.F.R. § 42.121. Accordingly, we grant the Motion to Amend to the extent it requests to cancel claims 4–6 and 10–12, and address below whether any of proposed substitute claims 13 and 14 have been shown to be unpatentable.

*C. Asserted Grounds of Unpatentability*

Petitioner asserts that the proposed substitute claims are unpatentable on the following grounds:

| Claims Challenged | 35 U.S.C. § | Reference(s)/Basis |
|---|---|---|
| 13, 14 | 103(a) | Smith |
| 13, 14 | 103(a) | Smith, Kigami |
| 13, 14 | 103(a) | Smith, Uemoto |
| 13, 14 | 103(a) | Sheu,[10] Kigami |

[10] TW200414540A, published August 1, 2004. Exs. 1035, 1036 (certified translation, "Sheu").

| Claims Challenged | 35 U.S.C. § | Reference(s)/Basis |
|---|---|---|
| 13, 14 | 112, ¶ 1 (enablement) | |

*D. Claims 13 and 14 in View of Smith, Smith/Kigami, and Smith/Uemoto*

Petitioner contends the subject matter of proposed substitute claims 13 and 14 would have been obvious in view of the disclosures of Smith, Smith/Kigami, and Smith/Uemoto. Opp. 22–35.

1. *Analysis—Proposed Substitute Claim 13*

Petitioner contends Smith teaches or suggests every limitation of proposed substitute claim 13 and would also render the claimed subject matter obvious when combined with either Kigami or Uemoto. Opp. 22–33. In support of its arguments, Petitioner provides the following annotated version of Figure 2A of Smith (Opp. 27).

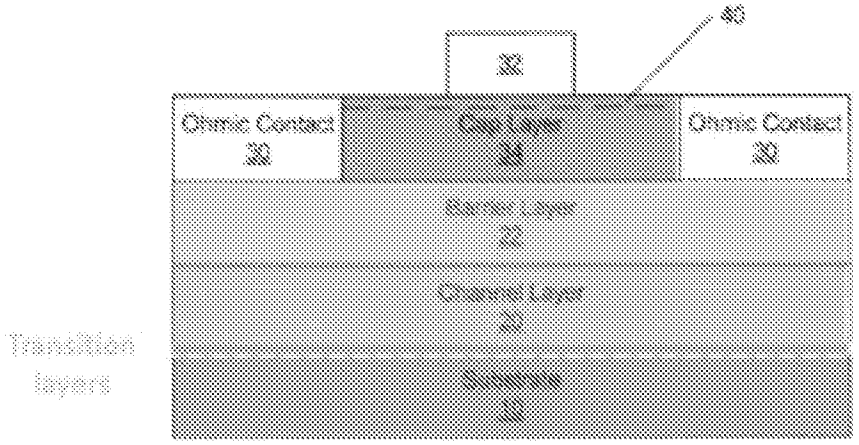



Figure 2A

Figure 2A, above, is annotated to show cap layer 34 in purple, barrier layer 22 in blue, channel layer 20 in green, the set of transition layers as a dashed yellow line, and substrate 10 in red. With respect to proposed substitute

claim 13, Petitioner contends that Smith teaches or suggests a substrate 10 (Opp. 24–25), a set of transition layers (*id.* at 25 (citing Pet. 35–36; Ex. 1039 ¶ 91)), a III-N buffer layer above the set of transition layers in the form of channel layer 20 (*id.* at 25–26), a III-N barrier layer above the buffer layer in the form of barrier layer 22 (*id.* at 26), a semi-insulating layer above the buffer layer in the form of cap layer 34 (*id.* at 26–28), and a gate contact 32 that is above cap layer 34 (*id.* at 30). With respect to the preamble, Petitioner contends that the transistor of Smith is an enhancement mode device because cap layer 34 contains p-type dopants and is below the gate and above the AlGaN layer. Opp. 24.

With respect to the requirement "wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen," Petitioner contends cap layer 34 of Smith has naturally present hydrogen that would form a "compensated GaN layer" and, to the extent the GaN layer of Smith is not passivated, one of ordinary skill in the art would have sought to do so in view of the knowledge of one of ordinary skill in the art, as well as the disclosures of Kigami and/or Uemoto. Opp. 29–30 (asserting that a person of ordinary skill in the art would have been "motivated to implement *Kigami*'s and *Uemoto*'s methods of using hydrogen to passivate and control active dopant concentrations in *Smith*'s device and reduce gate leakage"), 32.

With respect to the requirement for "a gate comprising a gate contact and the compensated GaN layer, wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias," Petitioner contends that because the device of Smith is an enhancement-mode device, there is no 2DEG under the gate at zero volts applied gate bias. Opp. 31–32. Petitioner further contends that one of ordinary skill in the art

applying known hydrogen-passivation methods, such as those disclosed in Kigami or Uemoto, would have ensured that enough active dopants are retained to deplete the 2DEG layer. *Id.* at 32.

Patent Owner contends that proposed substitute claim 13 would not have been obvious in view of Smith, Smith/Kigami, or Smith/Uemoto because (a) Smith does not disclose an "enhancement mode" transistor "wherein no two dimensional gas (2DEG) region exists below the gate at zero volts applied gate bias," (b) it would not have been obvious to form such a transistor in view of the disclosures of Smith, Kigami, and/or Uemoto, and (c) Smith does not disclose a semi-insulating III-N layer that comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen. Mot. Reply 12–17. We address the first two arguments below, as they are dispositive.

a. *Enhancement Mode Transistor with no 2DEG Region Below the Gate*

*1. Is Smith an Enhancement Mode Device?*

Dr. Shealy testifies that Smith discloses many different embodiments and variations within its transistors and contends one of ordinary skill in the art would have understood that the transistor of Figure 2A in Smith "can operate in enhancement-mode with the appropriate composition, doping, and thickness [selected] for its layers." Ex. 1033 ¶¶ 44–67; Ex. 1039 ¶¶ 88–89. Dr. Shealy further testifies that region 40 in Figure 2A is doped with p-type dopants and Smith discloses that this doping should be "sufficiently high so as to reduce gate leakage currents in embodiments without a recessed gate and be the dominant 'surface' state but not so high as to provide introduce [sic] traps or leakage paths by becoming a conductive layer." Ex. 1033 ¶ 51 (quoting Ex. 1005 ¶ 87). Dr. Shealy also testifies that Dr. Schubert admitted

that "if a p-type gate material is present over the barrier layer, it can deplete the 2DEG under the gate to create an enhancement mode" device. *Id.* ¶ 52 (quoting Ex. 2009 ¶ 31). Thus, Petitioner contends that the transistor in Figure 2A of Smith is an enhancement mode transistor, which would have no 2DEG below the gate at zero volts applied gate voltage. Opp. 24 (citing Ex. 1033 ¶¶ 46–59; Ex. 1039 ¶¶ 88–89; Ex. 1005 ¶¶ 14, 17, 85–87), 31–32.

We are not persuaded by this argument. Petitioner identifies no disclosure in Smith that its transistor operates as an enhancement mode device, and Petitioner never quantifies the level of p-type doping necessary in cap layer 40 of Smith to completely deplete the 2DEG at zero volts applied gate bias, while at the same time retaining the non-conductive nature of cap layer 40 (as disclosed in Smith). Mot. Reply 14 ("Petitioner has provided no evidence that acceptor-type dopants present in Smith's cap layer in fact cause the 2DEG beneath the gate to be depleted at zero volts applied gate bias."). And, although a p-type doped GaN layer under the gate and above the barrier layer *can* deplete the 2DEG under the gate, the evidence of record is clear that not just any p-type doped GaN layer will completely deplete the 2DEG at zero volts applied voltage. Opp. 10 ("But to deplete the 2DEG for an enhancement mode device requires sufficient active (unpassivated) acceptors."), 11–12 ("Without any guidance in the patent, determining active acceptor concentration necessary to deplete the 2DEG would require undue experimentation."); Mot. Reply 7 (asserting that the "Mg acceptor concentration should have a high level of doping to deplete the 2DEG").

In view of the foregoing, Petitioner has not demonstrated by a preponderance of the evidence that Smith, unmodified by any further

teaching or reference, teaches or suggests an enhancement mode device in which no 2DEG exists under the gate at zero volts applied voltage.

*2. Would Smith be Modified to be Enhancement Mode?*

Petitioner contends that enhancement mode devices were well known in the art and, to the extent Smith is not an enhancement mode device, one of ordinary skill in the art would have selected the appropriate p-type doping level necessary to arrive at an enhancement mode device. Opp. 31–32. First, Petitioner contends that one of ordinary skill in the art "would have identified doping concentration and layer thickness that result in enhancement mode devices even with natural passivation given *Smith*'s disclosures of ranges of these variables." *Id.* at 31 (citing Ex. 1039 ¶ 113; Ex. 1005 ¶¶ 77, 87). Second, Petitioner contends that Kigami and Uemoto describe techniques for localized hydrogenation of GaN layers and that this technique would reduce gate leakage. *Id.* at 31–32. According to Petitioner, "[w]hen passivating with hydrogen to reduce gate leakage with well-known methods, a [person of ordinary skill in the art] would have maintained an active dopant concentration that depleted the 2DEG." *Id.* at 32. One of ordinary skill in the art "would have done so," argues Petitioner, in order "to realize the benefits of enhancement mode devices, including reduced power consumption and suitability for high power applications," as disclosed in Suh2006.[11] *Id.* at 32.

Patent Owner contends there is no teaching in Kigami or Uemoto that would have motivated one of ordinary skill in the art to modify Smith's

[11] C.S. Suh, et. al., *P-GaN/AlGaN/GaN Enhancement Mode HEMTs*, 2006 64th Device Research Conference, June 2006, pp. 163–164. Ex. 1038 ("Suh2006").

depletion mode transistor to form an enhancement mode transistor, and Petitioner's reliance on Suh's 2006 article is "pure hindsight." Mot. Reply 16–17 (citing Ex. 2024 ¶¶ 45–46). Patent Owner further contends that any attempt to form an enhancement mode device in the embodiment depicted in Figure 2A of Smith would fail. *Id.* at 14–15. Patent Owner reasons that Figure 2A of Smith shows p-doped region 40 extending all the way between the source and drain, which would result in an extremely poor, if not inoperable, enhancement mode device. Mot. Reply 13; PO Resp. 25–30; Sur-reply 12–13; Ex. 2013, 62:12–63:12 (explaining that a conductive cap layer that extends between the source and drain "would be a disaster"). Patent Owner further reasons that, even if a small gap were provided between cap layer 34 and ohmic contacts 30, "[b]ecause the access regions are significantly wider than the small gaps between the cap layer and ohmic contacts, they would remain depleted of free electrons, and the transistor would be inoperable." Mot. Reply 13.

To explain its arguments, Patent Owner provides the following annotated figure:

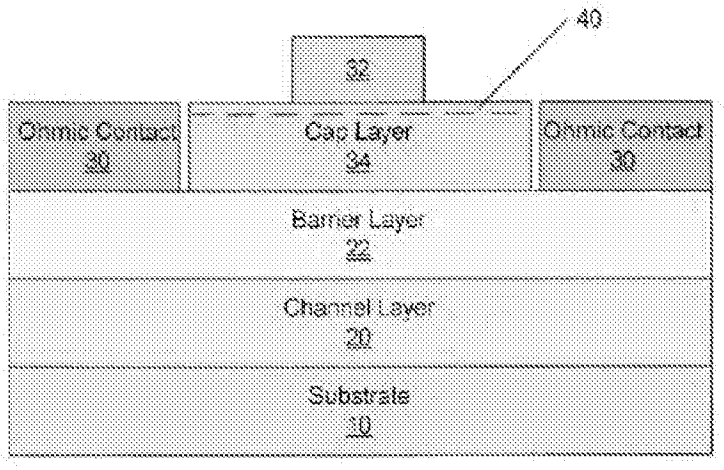



Figure 2A

Figure 2A, above, has been modified by Patent Owner to depict a small gap between cap layer 34 and ohmic contacts 30. Mot. Reply 13. Patent Owner contends that, to the extent the doping level of region 40 is sufficient to deplete the 2DEG, it would deplete the 2DEG under the entirety of cap layer 34, and when a voltage is applied to gate 32, the 2DEG would be reconstituted only under the gate 32. Mot. Reply 13–14. And, because electrons could not flow in the regions that are below the cap layer but not below the gate, Patent Owner contends the transistor would be inoperable. *Id.* at 13.

Petitioner contends Figure 2A of Smith is a "cartoon[]," and nothing in Smith requires "small gap[s]" as drawn by Patent Owner, with larger gaps being consistent with Smith's descriptions of its cap layer. Mot. Sur-reply 14. Petitioner further contends that Patent Owner is incorrect that the "2DEG is not replenished only below the gate because 'the electrical field would not be limited to below the gate.'" *Id.* at 14–15 (citing Ex. 1033 ¶¶ 57, 65–67).

Figure 2A depicts direct contact between ohmic contacts 30 and cap layer 34, and neither the Petition nor the Opposition suggests specific modifications to the structural design of cap layer 34 relative to Figure 2A. Moreover, contrary to Petitioner's arguments, Smith appears to specifically contemplate the configuration shown in Figure 2A and discussed by Patent Owner. For example, in discussing the formation of a Junction HEMT, Smith discloses that "[i]n such a case, the dope region 40 would not extend to the ohmic contacts 30," and may be isolated by a "SiN layer or gap." Ex. 1005 ¶ 88. Petitioner does not rely on this JHEMT embodiment and this disclosure suggests that in the other embodiments doped region 40 does in fact extend to the ohmic contacts 30, as specifically depicted in Figure 2A.

Patent Owner and Dr. Schubert persuasively testify that given this configuration, Smith would either not operate as an enhancement mode device, or its performance would be so poor that one of ordinary skill in the art would not have sought to modify Smith to create such a device.[12] Mot. Reply 12–13; Pet. Reply 25–26 (citing Ex. 2009 ¶ 117; Ex. 2024 ¶ 34; 2013, 62:12–63:12).

To the extent there is a gap between cap layer 34 and ohmic contacts 30, Patent Owner persuasively argues that such a device would either not act as an enhancement mode device, or would require such a significant level of voltage to operate that one of ordinary skill in the art would not have sought to use such a configuration. Mot. Reply 15. During an ITC evidentiary hearing, Petitioner's expert Dr. Michael Lebby testified that the 2DEG would ordinarily be reconstituted only under the gate, but by sufficiently increasing the voltage, one could reconstitute the 2DEG between the source and drain. Ex. 2016, 938:1–24[13]; Mot. Reply 15. Dr. Lebby had not modeled or simulated such an approach, however, and testified that such a device would "not be an ideal device" due to "lots of leakage." Ex. 2016, 938:25–939:8 (noting that it "[m]ay not be the best device, but you can make

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[12] Dr. Shealy testified that if doped region 40 in Smith (or Saxler) were conductive, "it would be a disaster." Ex. 2013, 62:12–23. As noted by Petitioner, however, Smith's doped region 40 is not conductive. Ex. 1005 ¶ 87. Regardless, Dr. Shealy testified that without a gap between cap layer 34 and the ohmic contacts, there would be "shunt problems." Ex. 2013, 65:12–18.

[13] Dr. Lebby's testimony related to U.S. Patent Application Pub. No 2006/0145189 A1 (Ex. 1040, "Beach189") and not Smith. It is undisputed, however, that similar to the device in Beach189, the 2DEG below cap layer 34 of Smith would be depleted at zero volts applied gate bias. Ex. 2009 ¶¶ 120–121.

it work."). Dr. Shealey agrees with Dr. Lebby's testimony, although he also does not provide any modelling or simulation to confirm such an approach would work, and contends that one of ordinary skill could have selected the conditions necessary to reconstitute the 2DEG from the source to drain in Smith, such as an appropriate applied gate voltage and drain voltage. Ex. 1033 ¶¶ 65–67.

Petitioner's Opposition does not assert that the device depicted in Figure 2A of Smith would be modified to introduce a gap between doped layer 40 and the ohmic contacts 30, or that the device would be modified to change the relative sizes and orientations of the ohmic contacts 30, cap layer 34, or gate 32. Opp. 22–33. Nor does Petitioner provide a persuasive explanation as to how precisely Smith would be modified to retain its desired function(s) and operate as an enhancement mode device. Thus, we credit the testimony of Dr. Schubert that the device of Figure 2A of Smith would either not act as an enhancement mode device, or would require such a significant level of voltage to operate that one of ordinary skill in the art would not have sought to use such a configuration. Ex. 2009 ¶¶ 122–123.

To the extent that the device of Figure 2A could be a viable enhancement mode device, Petitioner also fails to persuasively explain why one of ordinary would have modified Smith to passivate its p-type dopants. Smith adds p-type dopants to cap layer 34 to achieve specific results, i.e., to reduce leakage current and be the dominant "surface" state. Ex. 1005 ¶ 87. Petitioner's proposed combination with Smith, or Smith in combination with Kigami or Uemoto, would immediately passivate the very p-type dopants Smith intentionally added. Opp. 30. We are directed to no disclosure in Kigami or Uemoto of passivating p-type dopants that were intentionally added to provide a specific electrical property in the target layer. For

example, in Uemoto hydrogen is used to passivate Mg in region 15b because the electrical effects of this p-type dopant were not desired. Ex. 1006 ¶ 63. Likewise, in Kigami hydrogen passivation is used to inactivate all the p-type dopants in the local region 34, but not in region 32. Ex. 1008 ¶ 26, Figs. 1, 5. In both situations, the electrical effects of the added p-type dopants were not desired in a particular region, whereas in Smith the electrical effects of the added p-type dopant are desired. Petitioner does not persuasively explain, absent hindsight reasoning and knowledge of the claimed invention, why one of ordinary skill in the art would have sought to passivate the very p-type dopants that were desired in the reference. PO Resp. 38; Mot. Reply 15–16; PO Sur-reply 16. Thus, although hydrogen passivation was known in the art, and some level of natural passivation exists in the as-grown GaN layer of Smith, we credit the testimony of Dr. Schubert and find that Petitioner has not persuasively demonstrated that one of ordinary skill in the art would have actively passivated the p-type dopants of Smith that were added in specific amounts to "cause desirable effects, including reduc[ed] leakage currents." Ex. 2009 ¶¶ 141–142.

In view of the foregoing, Petitioner does not demonstrate by a preponderance of the evidence that the subject matter of proposed substitute claim 13 would have been obvious in view of Smith, or Smith in view of Kigami or Uemoto.

2. *Claim 14*

To support its arguments regarding proposed substitute claim 14, Petitioner relies on the device depicted in Figure 3B of Smith. Opp. 33. Petitioner's substantive arguments with respect to this device, however, are the same as those discussed above with respect to proposed substitute claim

13. *Id.* at 33–35. Thus, in view of the discussion of proposed substitute claim 13 above, we determine that Petitioner does not demonstrate by a preponderance of the evidence that proposed substitute claim 14 would have been obvious in view of Smith, or Smith in combination with either Kigami or Uemoto.

*E. Claims 13 and 14 over Sheu and Kigami*

Petitioner contends the subject matter of proposed substitute claims 13 and 14 would have been obvious in view of the combined disclosures of Sheu and Kigami. Opp. 35–49.

1. *Sheu*

Sheu discloses a field effect transistor with a GaN-based gate insulating layer. Ex. 1036, 3. Figure 6 of Sheu is reproduced below:

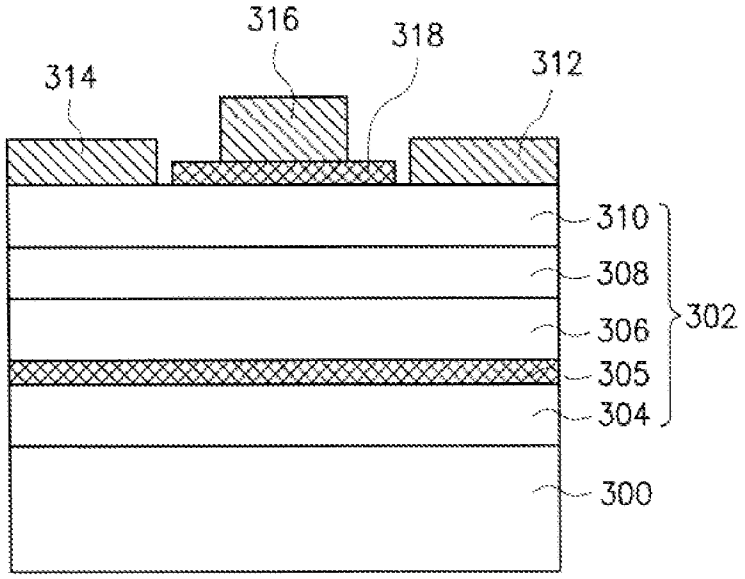


FIG. 6

Figure 6 "shows a structural schematic diagram of a field effect transistor according to a third exemplary embodiment" of Sheu. *Id.* at 10. As shown in Figure 6, the transistor is composed of gallium nitride substrate 300, GaN-

based semiconductor layer 302, GaN-based gate insulating layer 318, source 312, drain 314, and gate 316. *Id.* at 9. GaN-based semiconductor layer 302 is composed of, for example, buffer layer 304, isolation layer 305, channel layer 306, gap layer 308, and barrier layer 310. *Id.* at 9–10. The buffer and the channel layer may each be composed of an undoped $Al_aIn_bG_{a1-a-b}N$ layer with $a \geq 0$, $b \geq 0$, $1 \geq a+b$, and $x > a$. *Id.* at 10. Insulating layer 318 may be doped with, for example, carbon, magnesium, iron, or a combination of these materials, to enhance its resistance value. *Id.*

2. *Kigami*

Kigami discloses a semiconductor device that contains a p-type impurity wherein the concentration of the activated p-type impurity is locally adjusted to be low. Ex. 1008 ¶ 1. Kigami explains that one technique for forming a switching semiconductor device includes forming a gate electrode that is opposed, through an insulating film, by a semiconductor that contains a p-type impurity. *Id.* ¶ 4. "In this situation, there is a demand to lower the concentration of the p-type impurity contained in the semiconductor," as the region opposing the gate electrode "becomes easy to invert, and thereby the gate voltage required to turn the switching semiconductor device ON and OFF can be made small." *Id.* "[O]n the other hand, there is also a demand to raise the concentration of the p-type impurity" "because, when the concentration of the p-type impurity is lowered, the withstand voltage of the switching semiconductor device decreases." *Id.*

Kigami explains that "[t]he region in which it is desired to lower the concentration of the p-type impurity . . . is a local region that opposes the gate electrode" and the "region in which it is desired to raise the

concentration of the p-type impurity in order to increase the withstand voltage is the entire region of the semiconductor." Ex. 1008 ¶ 4. Kigami notes, however, that "in actuality, it is difficult to obtain a III-V group compound semiconductor in which the concentration of a p-type impurity is lowered locally." *Id.* ¶ 5.

Kigami explains that hydrogen atoms will inactivate p-type impurities in III-V group semiconductors. Ex. 1008 ¶ 7. Kigami utilizes this phenomenon to locally lower the concentration of the activated p-type impurity in the region opposing the gate electrode, while retaining sufficient activated p-type impurities in the majority of the III-V group compound semiconductor. *Id.*

Figure 1 of Kigami is reproduced below.

FIG. 1

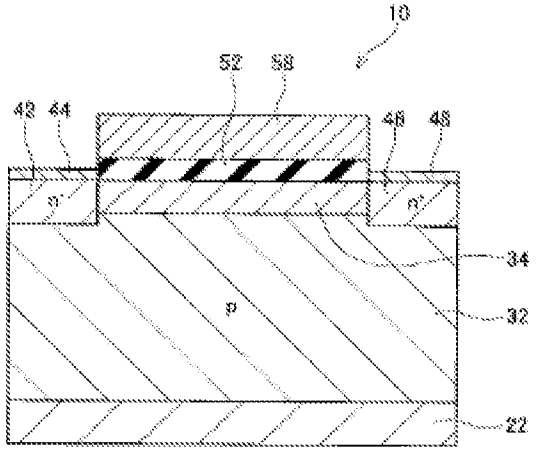


Figure 1 "schematically shows a longitudinal, cross-sectional view of the principal parts" of the semiconductor device. Ex. 1008 ¶ 38. As shown in Figure 1, semiconductor device 10 has a substrate 22, GaN layer 32, gate insulating film 52, gate electrode 58, source region 42, and drain region 46. *Id.* ¶ 20. A magnesium dopant is added to GaN layer 32 and then an ionized hydrogen gas is introduced to the front-surface side of GaN layer 32 to form

a local region 34 in which substantially all of the magnesium is inactivated. *Id.* ¶¶ 20, 22, 26. Kigami explains that "semiconductor device 10 has the characteristics of being able to operate at a low threshold voltage, having low loss, and having a high withstand voltage." *Id.* ¶ 23.

3. *Analysis—Proposed Substitute Claims 13 and 14*

Petitioner contends that the combination of Sheu and Kigami teaches or suggests every limitation of proposed substitute claim 13. Opp. 37–46. In particular, Petitioner contends that Sheu discloses a substrate (substrate 300) (element [13a][14]); a set of III-N transition layers (buffer layer 304 and isolation layer 305) that are above substrate 300 (element [13b]); a III-N buffer layer (channel layer 306 and gap layer 308) (element [13c]); and a III-N barrier layer (barrier layer 310) (element [13d]). Opp. 38–40. Petitioner concedes that Sheu does not disclose a "compensated GaN layer" that is a "semi-insulating III-N layer" (elements [13e.1] and [13e.2]), but contends such a layer would have been obvious in view of Kigami. *Id.* at 40–44. Petitioner reasons that gate insulating layer 318 of Sheu is p-type doped with magnesium to form an enhancement mode device and one of ordinary skill in the art would have sought to passivate some of these dopants using the hydrogenation technique of Kigami. *Id.* at 35–37, 41.

Petitioner contends one of ordinary skill in the art would have sought to passivate p-type dopants in Sheu for multiple reasons. First, Petitioner contends that Sheu and Kigami "both disclose III-nitride transistors and target the same problems of breakdown voltage and gate leakage." Opp. 36

[14] Petitioner's numbering of each element of proposed substitute claims 13 and 14 is provided in Appendix A to the Opposition. Opp. Appendix A: Claim Listing.

(citing Ex. 1039 ¶ 136). Second, Petitioner contends that Kigami teaches that its technique improves the characteristics of devices with magnesium dopants and Sheu also uses magnesium dopants to improve the same characteristics. *Id.* (citing Ex. 1039 ¶ 137; Ex. 1008 ¶¶ 12, 29; Ex. 1036, 10). Third, Petitioner contends that the use of Kigami's hydrogenation to locally passivate Sheu's GaN layer would represent the use of a known technique (Kigami's hydrogenation) in a known device (Sheu's transistor) that is ready for improvement. *Id.* at 37 (citing Ex. 1039 ¶ 140; Ex. 1008 ¶ 12; Ex. 1036, 10). According to Petitioner, one of ordinary skill in the art would have understood that Kigami's hydrogenation improves III-nitride transistors like Sheu's "by adjusting layer resistivity, controlling threshold voltage, enhancing breakdown voltage, and permitting high-frequency applications." *Id.* (citing Ex. 1008 ¶¶ 7, 8, 29).

Petitioner contends one of ordinary skill in the art would have expected to succeed in controlling the resistance of Sheu's layers using Kigami's hydrogenation method "because such passivation had been known for decades and *Kigami* adequately explains the passivation process and its effects." Opp. 37 (citing Ex. 1039 ¶ 141; Ex. 1008 ¶¶ 22–26).

We are not persuaded by Petitioner's arguments. First, Petitioner does not persuasively demonstrate that Sheu is directed to an enhancement mode device. Figure 4 of Sheu depicts the relationship between reverse bias voltage and gate leakage current in the transistors of Figures 1 and 3 of Sheu. Ex. 1036, Fig. 4. Dr. Schubert testifies that Figure 4 demonstrates that as voltage gets more negative, gate leakage current increases, which is consistent with a depletion mode transistor. Ex. 2024 ¶ 51; Mot. Reply 19. Dr. Schubert further testifies that gate insulating layer 318 is the same as that depicted in Figure 6 of Sheu and one of ordinary skill in the art would

understand the relationship between reverse bias voltage and gate leakage current to be the same in both embodiments. Ex. 2024 ¶ 51; Mot. Reply 19.

Patent Owner contends this conclusion is consistent with the findings from the related ITC investigation and a Chinese proceeding addressing the same subject matter. Mot. Reply 20; Ex. 2025, 33; Ex. 2019, 13. For example, in the Chinese proceeding it was determined that barrier layer 310 is doped n-type and, therefore, Sheu is a depletion mode transistor. Ex. 2019, 13 (addressing prior art reference D3). According to Patent Owner, because layer 310 is n-doped, the addition of p-type dopants discussed in Sheu would serve to increase the resistivity of the layer, not decrease it, as asserted by Petitioner. Mot. Reply 22 (citing Ex. 2024 ¶ 55). Likewise, in the ITC investigation, the pre-hearing brief of the Commission Investigative Staff stated that "Sheu discloses a depletion-mode field effect transistor." Ex. 2025, 32.

Petitioner contends that nothing in Sheu limits the device to depletion mode and one of ordinary skill in the art would have recognized that the combination of Sheu and Kigami "results in an enhancement mode device." Mot. Sur-reply 15–16 (citing Ex. 1039 ¶¶ 142–147, 188). Petitioner further contends that Patent Owner's speculation that "the gate insulating layer may be originally n-type" is not supported by the reference, which does not disclose any n-type doping of layer 318 and explicitly discloses that layer 318 is doped with p-type dopants, such as carbon, magnesium or iron. *Id.* at 16 (citing Ex. 1036, 10). And, according to Petitioner, a p-type gate material that is present over a barrier layer can deplete the 2DEG. *Id.* (citing Ex. 2009 ¶ 31; Ex. 1039 ¶ 189).

Dr. Schubert persuasively testifies that the plot of reverse gate voltage and gate leakage current in Figure 4 of Sheu is consistent with a depletion

mode device. Ex. 2024 ¶¶ 49–51. Petitioner does not persuasively address or refute this evidence. Moreover, although a p-doped GaN layer above a barrier layer *can* deplete the 2DEG, the evidence of record demonstrates that a semi-conductive or nonconductive compensated p-doped GaN layer below a gate contact will not always do so. Opp. 10; Mot. Reply 9. Thus, Petitioner does not persuasively demonstrate that Sheu is an enhancement mode device.

Second, to the extent Sheu were an enhancement mode device, Petitioner still has not established that the combination of Sheu and Kigami would render proposed substitute claims 13 and 14 obvious. It is undisputed that enhancement mode devices were known in the art, as was the use of hydrogenation to control the resistivity of p-doped III-N layers, such as a GaN layer. What is missing from the prior art presented by Petitioner is any understanding that a p-type doped GaN layer that is not conductive or is semi-conductive could be used to completely deplete the 2DEG under a gate electrode at zero volts applied gate bias. PO Resp. 1; Sur-reply 1.

The '294 patent discloses that conductive p-GaN layers were previously used in the art to create an enhancement mode device, but these prior art devices suffered from gate leakage and capacitance due to the conductivity of the GaN layer. Ex. 1001, 1:45–50, 3:43–52. Likewise, Suh2006 discloses a p-GaN layer that is doped to a level of $1x10^{18}$ $cm^{-3}$, and we are directed to no suggestion in the reference of using a non-conductive or semi-conductive p-GaN layer to completely deplete the 2DEG under the gate. Ex. 1038, 1. Thus, there is no persuasive evidence to refute the '294 patent's assertion that the enhancement mode devices of the prior art used a conductive layer under the gate to deplete the 2DEG and provide an enhancement mode device. PO Resp. 1 (asserting that "none of the asserted

prior art remotely suggests a transistor with a compensated gate" that allows enhancement mode operation).

Absent some understanding in the art that a compensated p-GaN layer that is semi-conducting or nonconductive could be used to deplete the 2DEG under the gate and form an enhancement mode device, Petitioner's arguments about fine tuning the p-doping and hydrogen content in Sheu and Kigami appear to be a hindsight attempt to reconstruct the claimed invention. Indeed, even if one of ordinary skill in the art were motivated to passivate some p-type dopants in Sheu using Kigami's method, Petitioner argues that it is difficult to find the precise balance where sufficient p-type dopants are present in the GaN layer to deplete the 2DEG under the gate but the remaining p-type dopants are sufficiently passivated to form a semi-conducting layer. Opp. 12–13, 15–16. Absent an understanding or evidence that a compensated, semi-conductive GaN layer could both completely deplete the 2DEG under the gate at zero volts applied gate bias and reduce gate leakage, we are presented with insufficient argument or reasoning as to why one of ordinary skill in the art would have embarked on the experimentation necessary to determine the necessary balance between p-type doping and hydrogen passivation in Sheu's device.

In view of the foregoing, Petitioner has not demonstrated by a preponderance of the evidence that proposed substitute claims 13 and 14 would have been obvious in view of Sheu and Kigami.

*F. Enablement of Proposed Substitute Claims 13 and 14*

Petitioner contends that claims 13 and 14 are not enabled because one of ordinary skill in the art would have required undue experimentation to achieve the claimed invention. Opp. 9. Petitioner reasons that creating an

enhancement mode device using a compensated GaN layer requires balancing two competing effects. On the one hand, the GaN layer must contain a sufficient dopant concentration to deplete the 2DEG. *Id.* On the other hand, sufficient passivation is necessary to ensure the GaN layer is not conductive. *Id.* Petitioner also contends that layer thickness influences the insulating nature of the GaN layer when passivating with hydrogen, with a thicker layer more difficult to passivate "and thus more difficult to compensate." *Id.* at 10. Petitioner contends the '294 patent is silent with respect to these multiple competing parameters "and achieving the proposed combination of claims 13–14 would thus have required undue experimentation." *Id.* at 11.

Patent Owner contends some experimentation is acceptable and the specification of the '294 provides a reasonable amount of guidance as to the direction in which experimentation should proceed. Mot. Reply 8–9. In particular, Patent Owner contends one of ordinary skill in the art would have understood from the disclosures of the '294 patent that sufficient acceptors must be present to deplete the 2DEG, and Patent Owner argues that determining this level would have been a routine procedure that cannot be characterized as "undue." *Id.* at 9. Patent Owner further contends that a person of ordinary skill in the art would have been able to identify the doping concentration, passivation level, and layer thickness required to result in an enhancement-mode transistor. *Id.*

Upon review of the prior art of record and the parties' arguments, we are not persuaded that forming the enhancement mode devices recited in proposed substitute claims 13 and 14 would have required undue experimentation. It is undisputed that enhancement mode transistors were known in the art and that the doping level of a layer under the gate needed to

be sufficiently high to deplete the 2DEG under the gate. Ex. 1001, 1:45–56; Ex. 1038. It is also undisputed that using hydrogen to passivate active acceptors was a known method in the art. *See, e.g.*, Ex. 1008, 7. Given the *teachings of the '294 patent* that a semi-conductive compensated GaN layer (or semi-insulating layer) could be sufficiently doped to completely remove the 2DEG layer but remain semi-conductive, we credit the testimony of Dr. Schubert that one of ordinary skill in the art, using only routine experimentation, could "tune" the level of p-type dopants and hydrogen to form a semi-insulating, compensated GaN layer that could deplete the 2DEG under the gate to form an enhancement-mode transistor. Ex. 2024 ¶¶ 28–31.

As noted by Patent Owner, this conclusion is consistent with Petitioner's obviousness arguments. Mot. Reply 9. In its Opposition to the Motion to Amend, Petitioner contends that a person of ordinary skill in the art seeking to passivate a GaN layer with hydrogen to reduce gate leakage "with well-known methods," "would have maintained an active dopant concentration that depleted the 2DEG." Opp. 32. To the extent one of ordinary skill in the art could create an enhancement mode device using a compensated GaN layer given the knowledge of skill in the art, the disclosures of prior art patents, and the known techniques for localized passivation and resistivity control, we agree with Patent Owner and Dr. Schubert (the pertinent testimony of whom we credit) that this same ordinarily skilled artisan could use the disclosures of the '294 patent to form the claimed transistors without undue experimentation. Ex. 2024 ¶¶ 29–30.

For the reasons discussed above, Patent Owner's Motion to Amend is granted with respect to substitute claims 13 and 14.

## V. CONCLUSION[15]

For the foregoing reasons, we determine that Petitioner demonstrates by a preponderance of the evidence that claims 1–3 and 7–9 are unpatentable. Our conclusions are summarized in the following table.

| Claim(s) | 35 U.S.C. § | Reference(s)/Basis | Claim(s) Shown Unpatentable | Claim(s) Not Shown Unpatentable |
|---|---|---|---|---|
| 1–3, 7–9 | 103(a) | Smith[16] | | |
| 1–3, 7–9 | 103(a) | Smith, Kigami[17] | | |
| 1–3, 7–9 | 103(a) | Smith, Uemoto[18] | | |
| 1–3, 7–9 | 103(a) | Uemoto, Smith | 1–3, 7–9 | |
| **Overall Outcome** | | | 1–3, 7–9 | |

In summary with respect to the proposed substitute claims:

| Motion to Amend Outcome | Claims |
|---|---|
| Original Claims Cancelled by Amendment | 4–6, 10–12 |
| Substitute Claims Proposed in the Amendment | 13, 14 |

[15] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

[16] For the reasons set forth above, we do not address Petitioner's arguments with respect to the Smith. *See supra* Section III.G.

[17] For the reasons set forth above, we do not address Petitioner's arguments with respect to Smith and Kigami. *See supra* Section III.G.

[18] For the reasons set forth above, we do not address Petitioner's arguments with respect to Smith and Uemoto. *See supra* Section III.G.

| | |
|---|---|
| Substitute Claims: Motion to Amend Granted | 13, 14 |
| Substitute Claims: Motion to Amend Denied | |
| Substitute Claims: Not Reached | |

## VI. ORDER

For the foregoing reasons, it is:

ORDERED that Petitioner demonstrates by a preponderance of the evidence that claims 1–3 and 7–9 of the '294 patent are unpatentable; and

FURTHER ORDERED Patent Owner's non-contingent Motion to Amend requesting cancellation of claims 4–6 and 10–12 and entry of proposed substitute claims 13 and 14 is *granted*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2023-01381
Patent 8,350,294 B2

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